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A MODEL OF TECHNOLOGICAL PROGRESS IN THE MICROPROCESSOR INDUSTRY*

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This paper develops a model of technological progress in the microprocessor industry that connects the seemingly disparate engineering and economic measures of technological progress. Technological progress in the microprocessor industry is driven by the repeated adoption of higher quality vintages of capital equipment produced by the upstream semiconductor equipment industry. The model characterizes the optimal adoption decision of a microprocessor firm and the resulting rate of technological progress. In conjunction with parameters estimated using a new dataset of the microprocessor industry, the model suggests explanations for the acceleration in technological progress during 1990–2000 and the subsequent slowdown.

I. INTRODUCTION

A NUMBER OF STUDIES SEEKING TO EXPLAIN THE INCREASE in productivity growth in the U.S. economy during the second half of 1990's credit a central role to an acceleration in technological progress in the microprocessor industry.[1] The cause of the acceleration has been debated in many academic, industrial and policy forums.[2] The rate of technological progress

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[1] Jorgenson [2001] was the first to point out the importance of the microprocessor industry. See also Oliner and Sichel [2002a] and Gordon [2002].

[2] See for example the proceedings of the workshop on Measuring and Sustaining the New Economy (2002), organized by the Board on Science, Technology and Economic Policy.

in the microprocessor industry slowed down after 2000. There has been no convincing explanation of the acceleration or slowdown to date. Jorgenson [2001] points to the need for an economic model of technological progress in this industry to understand the cause of the acceleration.

The multifaceted nature of technological progress in microprocessors has generated a plethora of characterizations of technological progress in this industry. Engineers favor a description based on Moore's law—a statement made in Moore [1975] that the number of transistors on a semiconductor chip doubles every two years.[3] Scientists prefer the rate at which the physical dimensions of an individual transistor has gone down, which has decreased by a factor of roughly 0.7 every 2–3 years. Business analysts in the semiconductor industry resort to the rate at which the processing speed (also called performance) of microprocessors have increased, while economists use the rate at which price per quality unit of microprocessors have declined.[4] By incorporating choices over engineering variables like transistor size and number of transistors, alongside economic variables like price, quantity and time of new technology adoption, the model in this paper connects these disparate engineering and economic measures of technological progress.

The model also formalizes the commonly held notion in the industry that the key decision facing a microprocessor firm is when to adopt a new vintage of capital equipment. Once the adoption decision has been made, profit maximizing considerations dictate a clear choice of the size of transistor to use, the number of transistors to use, the processing speed and the price per quality unit. A contribution of this paper is the characterization of the adoption decision and the resulting time paths for the four variables. The optimal time to adopt new capital equipment is when the lag behind the best available capital equipment reaches a threshold value. This result has been previously obtained in other models of technology adoption, including Balcer and Lippman [1984], Dixit and Pindyck [1994], and Farzin, Huisman and Kort [1998].[5] The predictions of the model regarding the adoption policy and the time paths of the four measures of technological progress fit well with the empirical observations, which are outlined in section II. The importance of the adoption of new capital equipment

[3] A transistor is the basic electronic component in a microprocessor. See section II for more details. Moore [1965] predicted the number of transistors on a chip to double every year, which was later revised to doubling every two years in Moore [1975].

[4] Table II gives average growth rates for performance and price per quality unit.

[5] Although not directly related, this paper is in the spirit of Griliches [1957], who uses a model of technology adoption to understand the causes of variation in hybrid corn adoption patterns across different states in the U.S. during 1932–1956. In a similar vein, this paper uses a model of technology adoption to understand the cause of the acceleration and slowdown that occurred in the rate of technological progress in the microprocessor industry during 1971–2008. For a good survey of models of technology adoption, see Hoppe [2002].

highlights the fact that technological progress in microprocessors is driven to a large extent by innovations in the upstream semiconductor equipment industry.[6] Semiconductor equipment firms like Nikon, Canon, Applied Materials and ASML invent new generations of capital equipment which allows microprocessor firms like Intel and AMD to fabricate smaller transistors, enabling them to make higher performance microprocessors. The notion that the repeated adoption of higher quality vintages of capital equipment is the driver of technological progress in the microprocessor industry has been emphasized in Aizcorbe and Kortum [2005].

A distinguishing feature of this paper is that it models technology in the industry in more detail than is common in economic models. This more detailed incorporation of the technology turns out to be essential not only in connecting the various measures of technological change but also in understanding the causes of the acceleration and slowdown in technological progress in the industry. The detailed modeling of technology helps to separate out the contribution of the semiconductor equipment firms from that of microprocessor firms towards technological progress in the microprocessor industry. There have been many previous studies of the acceleration and slowdown, including Jorgenson [2001], Aizcorbe [2005], Aizcorbe, Oliner and Sichel [2008] and Flamm [2004]. The studies above characterize the rate of technological progress in terms of the rate at which price per quality unit has declined for microprocessors.[7] This approach however has the limitation, as noted in Aizcorbe, Oliner and Sichel [2008], that changes in prices brought about by changes in demand and competitive conditions can be mistakenly attributed to changes in the rate of technological progress. To overcome this problem, I use the notion of technological progress as the growth of microprocessor performance.[8] Performance, or processing speed, is a measure of how fast a microprocessor can execute software programs. Nordhaus [2001] gives a detailed description of the use of performance as a measure of technological progress in computing, and compares it with the hedonic price based approach.[9] The growth rate of microprocessor performance increased during 1990–2000 and decreased subsequently (see Figure 1).[10]

[6] Section II elaborates on this link between technological progress in the microprocessor industry and the adoption of new vintages of semiconductor equipment.

[7] The price per quality unit is estimated using hedonic regressions.

[8] Performance is the commonly used measure for comparing microprocessors in computer science. It is the reciprocal of the time that the microprocessor takes to execute a given set of software programs.

[9] Song [2007] and Gordon [2009] are two other papers that use microprocessor performance.

[10] The changes in the growth rate of performance is broadly consistent with the changes in the growth rate in price per quality unit mentioned in Grimm [1998], Aizcorbe [2006] and Aizcorbe, Oliner and Sichel [2008]. See Table II.

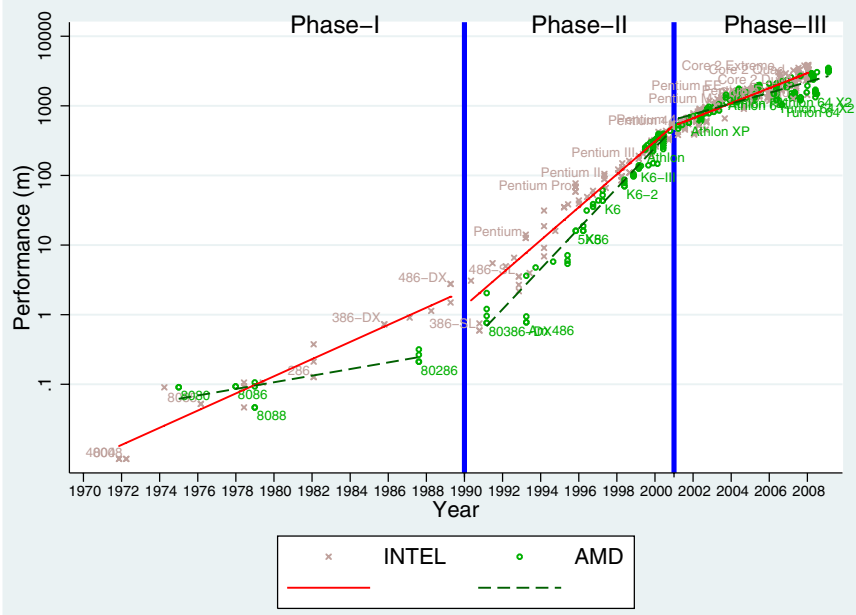

Figure 1
The Acceleration and Slowdown for Intel and AMD
Notes: The data on performance is obtained from two sources, SPEC and BAPCo. Both are industry consortia which develop benchmarks for measuring performance. Performance numbers in the graph are normalized by the performance of a standard microprocessor, and hence have no units.

The model in this paper implies that in steady state, the mean growth rate of performance is determined by two parameters. The first parameter is the rate of innovation in the upstream semiconductor equipment industry which determines the rate at which new capital equipment that can fabricate smaller transistors becomes available for adoption by microprocessor firms. The new equipment with smaller transistor size allows microprocessor firms to use more transistors in their microprocessor. The second parameter is the efficiency with which the microprocessor firm can convert the extra transistors to higher performance. This efficiency depends on the quality of microprocessor design (often called microarchitecture), a superior design can get a bigger increase in performance from a given increase in the number of transistors. The model, together with empirical estimates of the parameters, implies that the acceleration during 1990–2000 was caused by an increase in the innovation rate in the upstream semiconductor equipment industry, while the slowdown after 2000 was caused by a decrease in the efficiency with which the microprocessor industry used the upstream innovations in capital equipment.

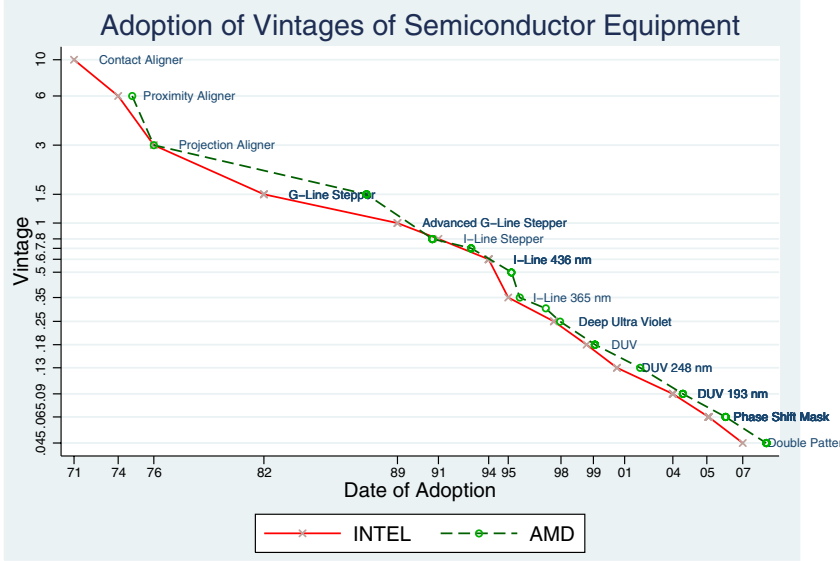

Figure 2
Intel and AMD's Adoption of New Vintages of Semiconductor Capital Equipment
Notes: The date of adoption of a vintage is taken to be the date on which Intel (or AMD) released the first microprocessor manufactured with that vintage. The dates marked on the x-axis are Intel's adoption dates. Note the decrease in the average time interval between adoptions after Phase I. This is the reduction in technology cycle that has been noted in Jorgenson [2001], Aizcorbe, Oliner and Sichel [2008] and Flamm [2004].

These explanations find support in other sources. Jorgenson [2001] suggests that the acceleration was caused by a decrease in the technology cycle in the semiconductor industry from three years to two years, a fact confirmed in Figure 2. An increase in the innovation rate in the semiconductor equipment industry leads to a decrease in the technology cycle, as shown in Section V of this paper. Aizcorbe, Oliner and Sichel [2008] also find support for an increase in the innovation rate in the semiconductor equipment industry. The decrease in efficiency, which led to the slowdown, occurred because after the early 2000's, microprocessor firms were not able to pursue the same approach as before to developing new microprocessor designs. During the 1990's Intel used a particular design approach starting with the Pentium and extending it to Pentium II, Pentium III and Pentium IV. However, with Pentium IV, the old design approach lead to an insurmountable engineering difficulty, the amount of heat created during the operation of microprocessors became too large and rendered the microprocessors

defective.[11] Since the early 2000's, microprocessor firms have developed a new design approach (the multicore design) which is not as effective in making use of transistors as the old design approach. Patterson [2010] provides a lucid account of the transition to the new design approach and the problems inherent in the new approach.[12] This technological explanation for the slowdown, acknowledged by the industry experts, has found its way even to the popular press, with the following quote coming from an article in the *The New York Times*. 'The computer industry has a secret. Yes, the number of transistors on modern microprocessors continues to multiply geometrically, but no one really knows how to get the most out of all these new transistors.'[13] To put it simply, the upstream equipment firms made available better capital equipment to microprocessor firms at a faster pace after 1990, but since 2000 the microprocessor firms have been unable to translate the improvements in capital equipment to improvements in performance at the same rate as before.

The slowdown since 2000 has reduced the contribution of the microprocessor industry to aggregate productivity growth. The impact of the acceleration and slowdown on total factor productivity (TFP) growth in the U.S. economy can be calculated using the method suggested in Oliner and Sichel [2002b]. In their method, the aggregate TFP growth is the weighted average of the TFP growth in the different sectors in the economy, where the weight for each sector is its gross output as a share of the aggregate output.[14] Using the growth rate of performance as a proxy for the TFP growth rate in the microprocessor industry, Table I shows that the contri-

[11] Markoff [2011] summarizes the problem: '. . . Now, however, researchers fear that this extraordinary acceleration is about to meet its limits. The problem is not that they cannot squeeze more transistors onto the chips—they surely can—but instead, like a city that cannot provide electricity for its entire streetlight system, all those transistors could require too much power to run economically. They could overheat, too . . .' 'I dont think the chip would literally melt and run off of your circuit board as a liquid, though that would be dramatic,' Doug Burger, an author of the paper and a computer scientist at Microsoft Research, wrote in an e-mail. 'But you'd start getting incorrect results and eventually components of the circuitry would fuse, rendering the chip inoperable'. . . . Shekhar Y. Borkar, a fellow at Intel Labs, called Dr. Burger's analysis right on the dot, . . . Chip designers have been struggling with power limits for some time. A decade ago it was widely assumed that it would be straightforward to increase chips' clock speed, or the rate at which it makes calculations. Then the industry hit a wall at around three gigahertz, when the chips got so hot that they began to melt. That set off a frantic scramble for new designs.' The article can be accessed at *http://www.nytimes.com/2011/08/01/science/01chips.html?pagewanted=all*.

[12] The article can be accessed at *http://spectrum.ieee.org/computing/software/the-trouble-with-multicore*.

[13] The quote appeared in an article titled 'Optimal Use of Transistors Still Elusive,' by John Markoff, in the September 1, 2009, release of *The New York Times*. The article can be accessed at *http://query.nytimes.com/gst/fullpage.html?res=9500E5DC1F38F932A3575AC0A96F9C8B63*.

[14] The theoretical justification for the method is given in Hulten [1978]. Note that this method captures only the direct contribution of production of microprocessors to aggregate TFP growth, and omits the indirect effect through the use of better computers made possible by faster microprocessors.

TABLE I
IMPACT ON AGGREGATE PRODUCTIVITY GROWTH

Phase	Output Share of Microprocessors (%)	TFP Growth in Microprocessor Industry (%)	Contribution of Microprocessors to Aggregate TFP Growth (% points)
1971–1989	0.06	28.4	0.017
1990–2000	0.14	50.2	0.070
2001–2008	0.13	22.9	0.031

Notes: The output share is obtained by multiplying the output share of semiconductors given in Oliner and Sichel [2002b] and Oliner, Sichel and Stiroh [2007] by a factor of 0.2, which is roughly the share of microprocessors in semiconductor industry revenue. The growth rate of performance is taken as a proxy for the TFP growth in the microprocessor industry. The entry in the fourth column is the product of the entries in the second and third columns. The fourth column represents only the direct contribution of the production of microprocessors to aggregate TFP growth; it ignores any indirect effect on aggregate TFP growth through the use of better computers made possible by faster microprocessors.

bution of the microprocessor industry to aggregate TFP growth quadrupled during the acceleration and more than halved during the slowdown. This paper suggests that technological progress in the microprocessor industry is unlikely to return to the accelerated path during 1990–2000, unless the industry finds a way to increase the efficiency with which it is using the innovations generated by the upstream semiconductor equipment industry. I now turn to a brief description of the connection between technological progress in the microprocessor industry and innovations in the upstream semiconductor equipment industry.

II. TECHNOLOGICAL PROGRESS IN MICROPROCESSORS

A microprocessor can be thought of as a collection of transistors which operate in tandem to execute instructions contained in different software programs. The performance of a microprocessor can be increased either by increasing the speed of operation of each individual transistor or by using more transistors so that more software instructions can be executed simultaneously (in parallel). The speed of operation of each individual transistor is limited by its size (smaller transistors are faster). The size of each transistor is in turn limited by the quality of the capital equipment used in manufacturing the microprocessor. Innovations in the semiconductor equipment industry lead to capital equipment that can make smaller transistors.[15] The evolution of the microprocessor industry towards faster

[15] The equipment industry has a separate classification under the North American Industrial Classification System (NAICS Code 333295). Some of the important firms in this industry are Applied Materials, Tokyo Electron, Nikon, Canon, ASML, Terdayne and Advantest. VLSI Research, a market research organization focusing on the semiconductor industry, estimates the total revenue for the equipment industry in 2007 to be 57.5 billion dollars, 67% of which was accounted for by the top 15 companies. (See *Semiconductor International* [2008].)

microprocessors traces the repeated adoption of higher quality vintages of capital equipment produced by the semiconductor equipment firms, each vintage of capital equipment being marked by the size (or length) of the transistor that the equipment allows the microprocessor industry to make. Since these transistor sizes are really small, they are usually quoted in microns (μ), which is a millionth of a meter.

The leading microprocessor firm, Intel, adopted fourteen such vintages during the years 1971–2008, 10μ, 6μ, 3μ, 1.5μ, 1μ, 0.8μ, 0.6μ, 0.35μ, 0.25μ, 0.18μ, 0.13μ, 0.09μ, 0.065μ and 0.045μ. Figure 2 plots the different vintages of semiconductor capital equipment that Intel and AMD have adopted against the date of adoption. In the progression through these fourteen vintages from 1971 to 2008, the transistor size has decreased by a factor of 222. I use the letter ℓ to denote the vintage of capital equipment which can produce transistors of size ℓ. A lower ℓ thus implies a higher quality vintage. I document below four stylized facts about the evolution of the four measures of technological progress in the microprocessor industry mentioned in the introduction. I denote the time period 1971–1989 as Phase

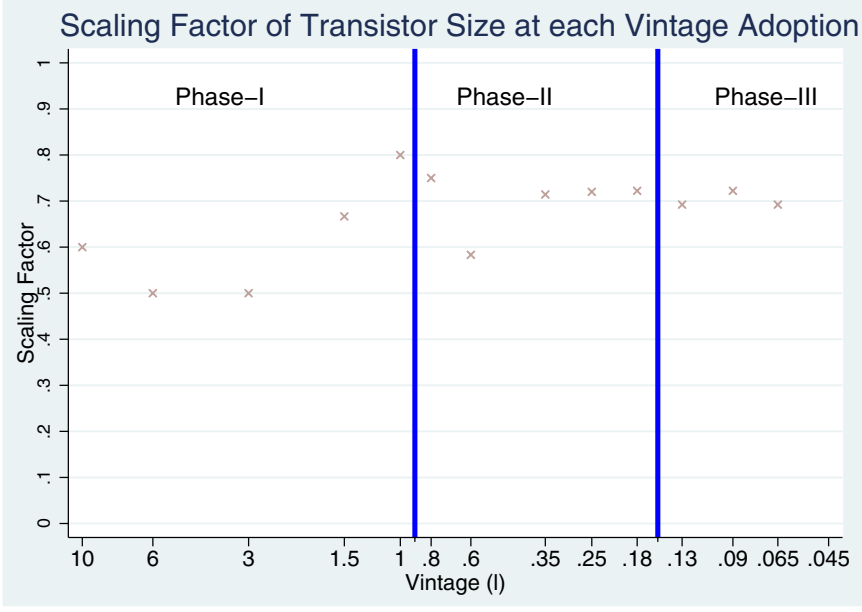

Figure 3
The Scaling Factor Does Not Show any Systematic Variation with ℓ

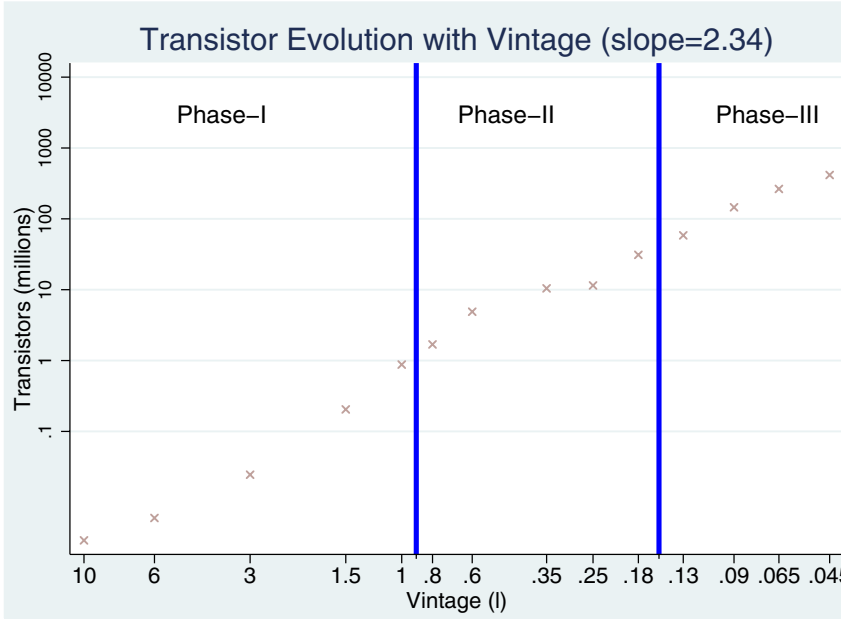

Figure 4
Transistors T Increase at Roughly Double the Rate at which ℓ Decreases. Note that x-axis Values Are Decreasing to the Right

I, the period 1990–2000 as Phase II and the period 2001–2008 as Phase III.[16] The four stylized facts are:

1. The adoption of each new vintage of capital equipment decreases the transistor size ℓ by roughly the same factor (see Figure 3). For brevity, I will call this the *scaling factor*.[17]
2. The number of transistors in a microprocessor, T, increases at roughly double the rate at which transistor size ℓ decreases (see Figure 4).
3. Performance, as measured by processing speed, grows at a roughly constant rate within each phase. The average growth rate of performance almost doubled going while from Phase I to Phase II (the acceleration) and more than halved while going from Phase II to Phase III (the slowdown). (See Figure 1 and Table II.)
4. Price/Performance (price per quality unit) declines at a roughly constant rate within each phase. The average decline rate of price/performance

[16] This section, and the other empirical sections of this paper, uses a new dataset of the microprocessor industry that has been created using data from a variety of sources. See Appendix for a description of the data sources.

[17] The scaling factor measures the size of the technological improvement that the new capital equipment provides at each adoption.

TABLE II
RATE OF TECHNOLOGICAL PROGRESS IN THE MICROPROCESSOR INDUSTRY

	Annual Performance Growth Rate (%)		
Company	1971–1989	1990–2000	2001–2008
Intel	28.4	50.2	22.9
AMD	10.9	65.4	18.5

Source: Author

	Annual Hedonic Price Index Decline Rate (%)		
	1986–1989	1990–1999	2001–2004
Microprocessor Industry	21	47	40.5

Source: Aizcorbe, Oliner and Sichel [2008], Aizcorbe [2006], Grimm [1998]
Notes: The top panel shows the average growth rate of microprocessor performance during the three phases. The bottom panel shows the rate of decline of price per quality unit, taken from Grimm [1998], Aizcorbe [2006] and Aizcorbe, Oliner and Sichel [2008]. As can be seen from the table, the growth of performance is broadly consistent with the declines in price per quality unit reported in previous studies. In the last phase, the difference likely arises from the difference in time periods.

increased while going from Phase I to Phase II (the acceleration) and decreased while going from Phase II to Phase III (the slowdown). (See Table II.)

Having motivated the role of innovation in the upstream equipment industry, the next section develops a model of how the upstream innovations percolate down and result in technological progress in the microprocessor industry that is consistent with the stylized facts above.

III. THE MODEL

The model is in continuous time. I develop the model in a few stages starting with the semiconductor equipment industry.

III(i). *The Semiconductor Equipment Industry*

Although the semiconductor equipment industry consists of a large number of firms which manufacture different types machinery, from the point of view of technological progress in the microprocessor industry the most important function that these companies serve is that they undertake the R&D necessary to manufacture the next vintage of capital equipment. Hence I lump all these companies together as the semiconductor equipment industry. I denote the frontier or highest quality vintage (i.e., the vintage with the smallest transistor size) by $\underline{\ell}$. The R&D done by the semiconductor equipment industry generates innovations that follow a Poisson process with parameter λ. Each innovation reduces $\underline{\ell}$ by a fixed factor δ, where $\delta < 1$. Hence the stochastic process for $\underline{\ell}$ can be written as

$$\overline{\ell}(t) = \delta^{N(t)}\overline{\ell}(0),$$

$N(t)$ *is a Poisson process with rate* λ.

I now turn to a description of the demand side of the model.

III(ii). *Demand in the Microprocessor Industry*

Consumers care only about the performance of microprocessors. I assume a stationary inverse demand curve, given by,

$$\frac{p(t)}{m(t)} = D(m(t)\,y(t))^{\frac{-1}{\eta}}, \tag{1}$$

where D is a parameter representing market size, $p(t)$ is the price of microprocessor sold at time t, $m(t)$ is the performance (quality) of the microprocessor and $y(t)$ is the number of microprocessors demanded. The price per quality unit is $\frac{p(t)}{m(t)}$, and $m(t)y(t)$ is the total number of quality units demanded. The basic assumption behind the demand structure is that total quality units demanded has a constant elasticity, η, in price per quality unit. One obvious abstraction in this demand specification is the absence of dynamic decision making by forward looking consumers.[18] It is unlikely that a change in dynamic decision making process by consumers could have been a cause of the acceleration and slowdown, so I ignore this aspect of demand. I now describe the technology side of the model.

III(iii). *Technology in the Microprocessor Industry*

A microprocessor firm like Intel chooses the quality (performance) of its product to maximize profits. The common way to model the quality choice of a firm is to have the firm pay a fixed cost to obtain an improvement in quality (e.g., in Sutton [2001]. The production process in the microprocessor industry, however, gives rise to a peculiar tradeoff between performance and costs not captured in such models. Equations (2) and (3) below, which capture the central aspects of production technology in the microprocessor industry, illustrate this tradeoff. A firm in the microprocessor industry has two ways to increase the performance of its microprocessor. First, it can adopt a new vintage of capital equipment which enables

[18] See Goettler and Gordon [2011] for a model of the microprocessor industry with forward looking consumers.

it to fabricate smaller (lower ℓ) and hence faster transistors.[19] Second, it can increase the number of transistors that it uses in its microprocessor, which allows the firm to fabricate more units working in parallel in the microprocessor, thus increasing performance.[20] Performance can thus be written as a function of the number of transistors T and the vintage of capital equipment ℓ,

$$m(T, \ell) = m_0 \frac{T^{\alpha}}{\ell}, \tag{2}$$

where m_0 is a constant. A microprocessor firm has the choice of increasing performance by increasing the number of transistors, without having to reduce ℓ by adopting a new vintage of capital equipment. Such an approach, however, increases the marginal cost of producing a microprocessor because it increases the fraction of microprocessors that are defective in any lot, a feature stemming from the peculiarities of the semiconductor production process. In any given lot of microprocessors manufactured, a certain fraction would be defective because of manufacturing imperfections arising from contamination by dust particles in the course of production. The fraction of defective microprocessors increases with the physical area A of the microprocessor because larger microprocessors have a higher probability of being contaminated by dust particles. A commonly used *yield* model in the industry gives the fraction of good microprocessors in any given lot as e^{-A}, where A is the area of the microprocessor.[21] Hence, if

[19] Reducing ℓ by a given factor increases the speed of each transistor by the same factor (see Ronen *et al*. [2000] or Borkar [1999]) and hence increases the performance m of the microprocessor by the same factor. 'Every new process generation brings significant improvements in all relevant vectors. Ideally, process technology scales by a factor of 0.7 all physical dimensions of devices (transistors) and wires (interconnects). . . . With such scaling, typical improvement figures are the following: 1.4–1.5 times faster transistors; two times smaller transistors . . . ,' Ronen *et al* [2000]. The names 'process generation' and 'process technology' in the above quote are terms used in the semiconductor industry to refer to vintages of capital equipment.

[20] The relationship between number of transistors and performance has come to be known in the semiconductor industry as Pollack's rule. Fred Pollack was a leading microprocessor designer at Intel in 1990's, who observed that a doubling of transistors allowed Intel engineers to build new microprocessor designs that had a roughly 40% increase in performance. This would imply an α of around 0.5. For a good reference on Pollack's rule, see Borkar and Chien [2011]. Pollack's rule is a rough rule of thumb and there can be variations in α depending on the quality of the design used in the microprocessor. In particular, Borkar and Chien [2011] mention that the new designs developed by Intel based on the multicore approach have not been able to deliver the same performance increases as predicted by Pollack's rule.

[21] The formula for the fraction good microprocessors (*yield*) used in this paper, e^{-A}, is called the Poisson yield equation. The Poisson yield is usually given as $e^{-\sigma S}$, where σ is a parameter that captures the degree of manufacturing imperfections, and S is the physical area of the microprocessor. For the purposes of this paper, $A = \sigma S$, can be thought of as the effective area, which takes into account the multiplication by σ. See Berglund [1996] for a description of yield models in the semiconductor industry.

$\bar{c}$ is the unit cost of producing a raw microprocessor, the marginal cost of producing a good microprocessor is $\bar{c}e^{A}$. Since the area of each individual transistor is ℓ^2, the area the microprocessor containing T transistors is $A = T\ell^2$. Substituting for A, the marginal cost is given by,

$$c(T, \ell) = \bar{c}e^{T\ell^2} \tag{3}$$

Increasing T without reducing ℓ rapidly escalates the marginal cost. If the firm reduces ℓ by adopting a new vintage and increases T in proportion to $\frac{1}{\ell^2}$, then the marginal cost remains constant while performance increases. This is indeed the policy that the model in this paper predicts to be the optimal policy, as well as the policy that microprocessor firms have followed in practice (see stylized fact 2 and Figure 4). Although adopting a new vintage allows a microprocessor firm to keep marginal cost constant while increasing performance, the firm has to expend a considerable amount of engineering effort in perfecting the production process with the new vintage of machines.[22] I capture this fixed cost with the function $F(\ell)$, which increases as ℓ decreases. The fixed cost $F(\ell)$ does not include the user cost of capital, which is incorporated into the unit cost of producing a raw microprocessor, $\bar{c}$.

The functions $m(T, \ell)$, $c(T, \ell)$ and $F(\ell)$ capture the technology in this industry. Note that in the function $m(T, \ell)$ in equation (2), the ability of a microprocessor firm to translate increases in T to increases in m depends on the parameter α. The parameter α is a measure of quality of design used in the microprocessor. With a superior design (higher α), a microprocessor firm can get bigger performance increments from a given increase in the number of transistors. This design quality is thus a measure of the technical *efficiency* of the microprocessor firm. In section V, I argue that a drop in efficiency α caused the slowdown in technological progress in the industry. Using the primitives of demand and technology in sections (III(ii)) and (III(iii)), the next section lays down the profit maximization problem faced by a microprocessor firm.

III(iv). *The Profit Maximization Problem of the Microprocessor Firm*

Before turning to a formal description of the microprocessor firm's problem, I make two assumptions. First, I assume that the market for microprocessors consists of a single firm facing the demand curve in equation (1). Although there are two major microprocessor producers, Intel and

[22] Intel has estimated the cost of adopting the vintage of capital equipment with $\ell = 0.032\mu$ to be 7 billions dollars. See Condon [2009].

AMD, Intel has been at the forefront of making innovations in the industry while AMD has usually lagged behind. Intel has also occupied 75%–90% of the microprocessor market during the time period considered in this paper. Moreover, in a paper exploring whether AMD spurs Intel to innovate, Goettler and Gordon [2011] find that innovation is more an Intel monopoly than an Intel-AMD duopoly. In the light of these arguments, modeling the industry as a duopoly would complicate the analysis while providing little help in finding explanations for the acceleration and slowdown.[23] Second, I assume that the microprocessor firm sells only the highest quality (performance) microprocessor. As soon as a better product is made, the entire production is moved to the new product. This assumption helps focus on the factors that determine the rate at which microprocessor performance is growing.

Given the Poisson arrival rate λ of innovations to capital equipment, each of which reduces $\overline{\ell}$ by a factor δ, the microprocessor firm has to choose the time paths of performance, marginal cost, the number of microprocessors to produce, the vintage of capital equipment to use, and the sequence of times at which to adopt new vintages of capital equipment, $\{\tau_j\}_{j=0}^{\infty}$. The choice of performance and marginal cost can equivalently be stated in terms of choice of the number of transistors and the vintage of capital equipment. Formally, the problem of the microprocessor firm is,[24]

$$\max_{T(t),\ell(t),y(t),\{\tau_j\}_{j=0}^{\infty}} \quad E\left[\int_0^{\infty} e^{-\rho t}[p(t)-c(T,\ell)]y(t)\,dt-\sum_{j=0}^{\infty} e^{-\rho\tau_j}F\left(\ell\left(\tau_j\right)\right)\right]$$

$$\text{subject to} \quad \frac{p(t)}{m(T,\ell)}=D(m(T,\ell)\,y(t))^{\frac{-1}{\eta}},$$

$$m(T,\ell)=m_0\frac{T^{\alpha}}{\ell},\ c(T,\ell)=\overline{c}e^{T\ell^2}$$

$$\ell(t)\geq\overline{\ell}(t),\quad \overline{\ell}(0)\text{ given},$$

$$\overline{\ell}(t)=\delta^{N(t)}\overline{\ell}(0),\ N(t)\text{ is a Poisson process with rate }\lambda.$$

[23] As can be seen in Figure (1), AMD started Phase II as a laggard and caught up with Intel towards the end of Phase II (see Figure 1). During Phase III, AMD again fell back behind Intel. Hence if competition from AMD does in fact reduce innovation by Intel (as has been found in Goettler and Gordon [2011]), then Intel should have had lower growth rate in performance in Phase II as compared to Phase III. This is the opposite of what is seen in the data. Hence if Goettler and Gordon [2011] is correct, change in competitive pressure between Intel and AMD cannot be the explanation for the acceleration and subsequent slowdown in growth rate of Intel's performance.

[24] To avoid notational clutter, I have abbreviated $m(T(t), \ell(t))$ as $m(T, \ell)$ and $c(T(t), \ell(t))$ as $C(T, \ell)$ in the statement of the problem.

The term in the outer square brackets is the present discounted value of net profits, which is the difference between the present discounted values of gross profits (the integral term in the objective function) and the sum of fixed costs of adopting new vintages (the summation term in the objective function). The first constraint is the demand curve in equation (1), the second and third are the technology constraints in equations (2) and (3), the fourth simply states that the firm can at best be using the best vintage currently available, and the last specifies the stochastic process for the evolution of the best (frontier) vintage. I restrict $\eta > 1$ to make the firm's problem well defined.

III(v). *Microprocessor Firm's Optimal Policies*

The optimal choice of T and y depend only on the current value of ℓ. Hence I solve the problem by first solving the static problem of choosing T and y for a given ℓ and then embedding this solution back into the problem, to solve the dynamic problem of choosing the optimal times $\{\tau_j\}_{j=0}^{\infty}$ at which to adopt new ℓ. Substituting the constraints into the objective function, it can be seen that the solution to the static problem is as follows. Along an optimal path of T and y, the following condition has to hold,

$$T^*(\ell) = \alpha \frac{1}{\ell^2}. \tag{4}$$

Substituting equation (4) into equation (3) gives marginal cost as

$$c^*(\ell) = \bar{c}e^{\alpha} \equiv c^*. \tag{5}$$

The firm's optimal policy is thus to choose T in proportion to $\frac{1}{\ell^2}$ and hence keep the marginal cost at $c^* = \bar{c}e^{\alpha}$, irrespective of the vintage ℓ used. The optimality conditions in equations (4) and (5) result from the tradeoff between performance and marginal cost explained in section III(iii). Substituting equation (4) into equation (2) gives the optimal performance as,

$$m^*(\ell) = m_0 \frac{T^*(\ell)^{\alpha}}{\ell} = m_0 \alpha^{\alpha} \frac{1}{\ell^{1+2\alpha}}. \tag{6}$$

i.e., performance grows at $1 + 2\alpha$ times the rate at which ℓ decreases. The term $1 + 2\alpha$ shows the twin benefits that a microprocessor firm gets from using a vintage with a smaller ℓ. The exponent 2α represents the indirect benefit of smaller ℓ on m through T, and the exponent 1 represents the direct benefit arising from the fact that smaller transistors are faster. The optimal number of microprocessors to produce $y^*(\ell)$ is,

$$y^*(\ell) = (\eta - 1)\frac{1}{\bar{c}e^{\alpha}}\frac{\pi}{\ell^{\varphi}}. \tag{7}$$

where π and φ are given by,

$$\pi = \left((\eta - 1)m_0 \frac{\alpha^{\alpha}}{\bar{c}e^{\alpha}}\right)^{\eta - 1}\left(\frac{D}{\eta}\right)^{\eta}, \tag{8}$$

$$\varphi = (1 + 2\alpha)(\eta - 1). \tag{9}$$

Substituting the solutions for m and y into the demand equation (1) gives the optimal price as,

$$p^*(\ell) = \frac{\eta}{\eta - 1}\left[\bar{c}e^{\alpha}\right] \equiv p^*, \tag{10}$$

i.e., the price of a microprocessor is a constant markup over the marginal cost of production, the term inside square brackets being the marginal cost of production. The solutions p^* and $y^*(\ell)$ give the revenue along the optimal path as

$$r^*(\ell) = \eta\frac{\pi}{\ell^{\varphi}}. \tag{11}$$

As expected for a constant elasticity demand curve, the gross profit is a constant fraction $\frac{1}{\eta}$ of revenue, and is given by,[25]

$$\pi^*(\ell) = \frac{\pi}{\ell^{\varphi}}. \tag{12}$$

Using the gross profit function in equation (12), the microprocessor firm's problem can be rewritten as

$$\max_{\ell(t),\{\tau_j\}_{j=0}^{\infty}} \quad E\left[\int_0^{\infty} e^{-\rho t}\pi^*(\ell(t))\,dt - \sum_{j=0}^{\infty} e^{-\rho\tau_j}F(\ell(\tau_j))\right]$$

$$\text{subject to} \qquad \pi^*(\ell(t)) = \frac{\pi}{\ell(t)^{\varphi}},$$

$$\ell(t) \geq \bar{\ell}(t),\ \bar{\ell}(t) = \delta^{N(t)}\bar{\ell}(0),$$

$$N(t) \text{ is a Poisson process with rate } \lambda.$$

[25] Note that π defined in equation (8) is equal to $\pi^*(1)$.

I solve the problem using dynamic programming. The dynamic programming problem is most conveniently expressed by choosing the state variables as $\bar{\ell}$, the frontier vintage, and $x = \frac{\bar{\ell}}{\ell}$, which captures how far the firm is behind the frontier. Note that $x \leq 1$, since the firm can adopt a vintage no smaller than $\bar{\ell}$. Since the innovation arrival is Poisson, the probability of one innovation arriving in a small interval of time Δt is $\lambda \Delta t$, and the probability of more than one innovation is approximately zero. Hence the value function should satisfy the Bellman equation,

$$V(\bar{\ell}, x) = \frac{\pi}{\left(\frac{\bar{\ell}}{x}\right)^{\varphi}} \Delta t + e^{-\rho \Delta t}\Big[(1 - \lambda \Delta t) V(\bar{\ell}, x) + \lambda \Delta t \, Max\{V(\delta \bar{l}, \delta x), V(\delta \bar{\ell}, 1) - F(\delta \bar{\ell})\}\Big].$$

The first term on the right hand side is the profit that the firm receives in a small interval of time Δt, the second term is the discounted expected payoff after Δt. With probability $1 - \lambda \Delta t$ no innovations arrive in which case the firm's value remains at $V(\bar{\ell}, x)$. With probability $\lambda \Delta t$ one innovation arrives, in which case the firm has to choose between not adopting this innovation and getting value $V(\delta \bar{\ell}, \delta x)$ or adopting it and getting a value $V(\delta \bar{\ell}, 1) - F(\delta \bar{\ell})$.

I assume that $F(\ell)$ is homogeneous of degree $-\varphi$, the same degree of homogeneity as the gross profit function, $\pi^*(\ell)$. If this were not true, then one would get a non-stationary model. If $F(\ell)$ were increasing at a faster rate in ℓ than $\pi^*(\ell)$, then the factor by which ℓ scales at each adoption (the scaling factor) would decrease over time, getting closer to 0. If $\pi^*(\ell)$ was increasing at a faster rate than $F(\ell)$, then the scaling factor would increase over time, getting closer to 1. However, as Figure 3 shows, the scaling factor does not show any systematic variation over time, consistent with the assumption that $F(\ell)$ is homogeneous of degree $-\varphi$. The assumption that $F(\ell)$ is homogeneous of degree $-\varphi$ implies that $V(\bar{\ell}, x)$ is homogenous of degree $-\varphi$ in $\bar{\ell}$, and hence $V(\bar{l}, x) = \bar{l}^{-\varphi} V(1, x) = \bar{\ell}^{-\varphi} v(x)$, where $V(1, x) = v(x)$. The dynamic program can thus be expressed with a single state variable, x. Re-writing with the single state variable, and taking the limit $\Delta t \to 0$, the Bellman equation simplifies to,

$$\rho v(x) = x^{\varphi} \pi + \lambda \left[\frac{1}{\delta^{\varphi}} Max\{v(\delta x), v(1) - F(1)\} - v(x) \right]. \tag{13}$$

The left hand side of the equation is the payoff to owning the firm, which is the sum of the instantaneous payoff and the change in value which occurs if an innovation arrives, an event with hazard λ (taking account of the

option to adopt). Proposition 1 characterizes the optimal adoption policy of the firm.

Proposition 1. The optimal policy of the firm is to wait until x falls below a threshold value x^*, where

$$x^* = \left\{\left(\rho + \lambda - \frac{\lambda}{\delta^{\varphi}}\right)\left(\frac{v(1) - F(1)}{\pi}\right)\right\}^{\frac{1}{\varphi}}. \tag{14}$$

See Appendix for proof.

Equation 14 can be rearranged to obtain,

$$\rho(v(1) - F(1)) = \pi x^{*\varphi} + \lambda\left\{\frac{1}{\delta^{\varphi}}[v(1) - F(1)] - [v(1) - F(1)]\right\}. \tag{15}$$

Equation (15) is the value matching condition mentioned in Dixit and Pindyck [1994] and Farzin, Huisman and Kort [1998]. The firm adopts at the point at which the value of adopting is equal to the value of waiting. The value of adopting immediately is the left hand side of the equation, the firm jumps to the frontier but it has to pay the fixed cost $F(1)$. The term on the right hand side is the value of waiting which is the sum of instantaneous payoff and the change in value that occurs if an innovation arrives at that moment in time. Note that equation (14) requires $\rho > \lambda\left(\frac{1}{\delta^{\varphi}} - 1\right)$.[26] Since each innovation shrinks $\overline{\ell}$ by δ, this implies that it is optimal to adopt at every n^*th innovation, where n^* is the smallest integer such that $\delta^{n^*} \leq x^*$. It is easy to summarize the dynamic policy using the simple diagram in Figure 5.

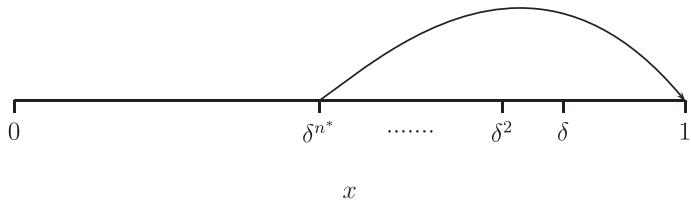

Figure 5
Adoption Policy of the Firm

[26] If discount factor ρ is not high enough, then discounted net profits are increasing over time and there will be no solution to the firm's problem.

The possible values of x are $1, \delta, \delta^2, \ldots, \delta^{n^*-1}$. Starting from $x = 1$, the value of x decreases to δ, δ^2,.., as the equipment sector produces its stream of innovations. When the n^*th innovation arrives, the firm adopts it and x becomes equal to one again. This cycle repeats.

I summarize the results above. The microprocessor firm adopts every n^*th innovation made by the semiconductor equipment industry and hence ℓ used by the firm scales repeatedly by the same factor δ^{n^*}. As ℓ decreases, the firm chooses to increase transistor count (T) and performance (m) in proportion to $\frac{1}{\ell^2}$ and $\frac{1}{\ell^{(1+2\alpha)}}$ respectively. The firm chooses to maintain the marginal cost at c^* and charge a price p^* per microprocessor, while increasing the number of units produced (y) in proportion to $\frac{1}{\ell^{\varphi}}$, where $\varphi = (1 + 2\alpha)(\eta - 1)$. Revenue and gross profits also increase in proportion to $\frac{1}{\ell^{\varphi}}$. This concludes the development of model.

IV. DISCUSSION

In this section I show that the model's predictions are consistent with the stylized facts documented in section II, and use the model to connect the four measures of technological progress mentioned in the introduction. The optimal choices of the firm with regard to engineering variables like number of transistors and performance, as well as economic variables like quantity, profits and revenue, are determined by the vintage ℓ of capital equipment that the firm is using, and evolves with the change in ℓ at each new vintage adoption. The model thus formalizes the commonly held notion in the microprocessor industry that the adoption of new vintages of capital equipment is the key driving force in the industry.

The model predicts that at the adoption of each new vintage, the transistor size ℓ should scale by the same factor δ^{n^*}, accounting for stylized fact 1. As equation (4) shows, the model predicts that the firm's optimal policy is to increase T in proportion to $\frac{1}{\ell^2}$, accounting for stylized fact 2. I show below that the mean growth rate of m is given by

$$g_m = -(1+2\alpha)\lambda \ln(\delta). \tag{16}$$

Thus the mean growth rate of m is constant as long as α and λ does not change. I argue in section V that changes in g_m between the three phases were caused by shifts in λ and α. Within each phase, with λ and α fixed, the model predicts that the mean growth rate of m is constant, accounting for stylized fact 3. Since price p does not change over time, the model predicts that price/performance ($\frac{p}{m}$) declines inversely with m, accounting for stylized fact 4. The model makes one more testable prediction, that the microprocessor firm should adopt only occasionally, and should skip some innovations. In Figure 6, I plot the vintages adopted by Intel (solid horizontal lines). The dotted lines are some of the vintages for which capital

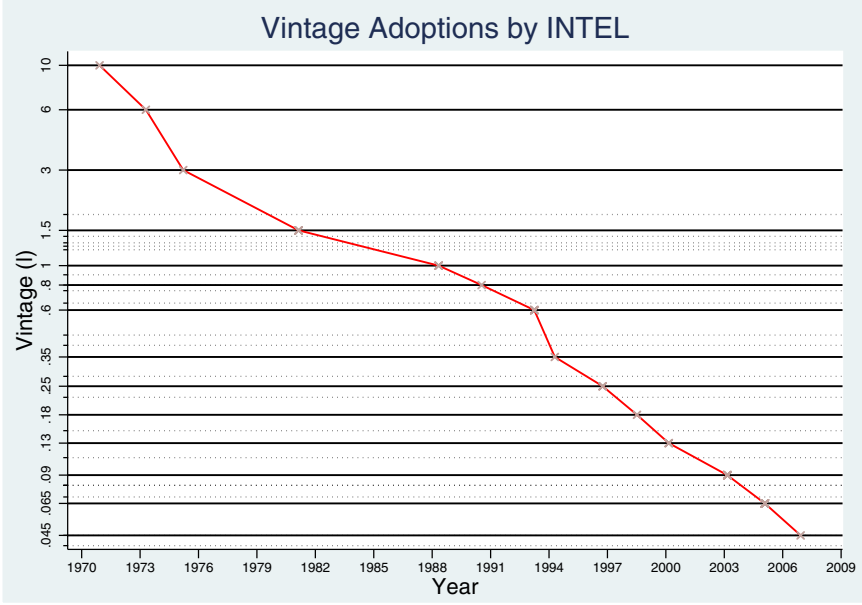

Figure 6
Intel Does Not Adopt all Vintages

Notes: The solid lines are vintages that were adopted by Intel. The dotted lines are vintages that were produced by semiconductor equipment firms but were not adopted by Intel. In line with the prediction of the model, Intel does not adopt all vintages produced by semiconductor equipment firms. The dotted lines are not the exhaustive list of all vintages, and correspond to only those vintages for which I could obtain data (from the websites of semiconductor equipment companies or from industry reports).

equipment was sold by some of the leading semiconductor equipment producers, but were not used by Intel.[27] As can be seen from the graph, there were quite a number of vintages which Intel did not adopt, in line with the prediction of the model.[28]

[27] The vintages for the dotted lines were produced by one of the following equipment companies—ASML, Nikon, GCA, SVGL, Parkin-Elmer and Ultratech.

[28] Although Intel does not adopt all vintages produced, the equipment firms have an incentive to innovate and produce these vintages because their customers include all companies that make semiconductor chips. In addition to microprocessor producer Intel, companies who buy semiconductor equipment include producers of memory chips (like Samsung, Micron and Hynix, Toshiba, Fujitsu), producers of semiconductor chips used in electronic devices (like Sony, Panasonic, Freescale, Fujitsu), as well as contract manufacturers of semiconductor chips (like Global Foundries, Taiwan Semiconductor Manufacturing Corporation, etc). These companies probably follow different adoption patterns, influenced by the market structure and profitability in their own segments. Data collected on semiconductor chips made by other companies (like Samsung) indicate that they have adopted vintages in the past which were not adopted by Intel.

The model connects the four measures of technological progress mentioned in the introduction. Since the firm's policy is to adopt every n^*th innovation, the mean growth rate of ℓ will be determined by the stochastic process generating the innovations. Proposition (2) gives the mean growth rate of ℓ.

Proposition 2. If the firm adopts every n^*th innovation, then the mean growth rate of ℓ *is* $g_\ell = \lambda \ln(\delta)$.[29]

See Appendix for proof.

From equation (4) it is clear that T increases at twice the rate at which ℓ decreases, i.e., $g_T = -2\lambda \ln(\delta)$. From equation (6) it follows that $g_m = -(1 + 2\alpha)g_\ell$. This gives the mean growth rate of m as, $g_m = -(1 + 2\alpha)\lambda \ln(\delta)$. Finally, since the price of a microprocessor remains constant over time, the price per performance decreases at the rate at which performance increases, i.e., $g_{pm} = (1 + 2\alpha)\lambda \ln(\delta)$. The four expressions above bring out the relationships between the four measures of technological progress in the industry. While the rate of reduction in transistor size (g_ℓ) and growth in number of transistors per microprocessor (g_T) is fixed by the innovation parameters λ and δ in the upstream semiconductor equipment industry, the rate of growth of performance (g_m) and price/perperformance (g_{pm}) depend also on the the efficiency α with which the microprocessor firm uses the upstream innovations.

V. EXPLANATIONS FOR THE ACCELERATION AND SLOWDOWN

In this section I use the model to study the acceleration and subsequent slowdown in technological progress, measured as growth of performance. I will argue below that the acceleration was caused by an unanticipated increase in the upstream innovation rate λ, and the slowdown by an unanticipated decrease in the efficiency α with which Intel used upstream innovations. These explanations are consistent with the model, since it can be seen from equation (16) that an increase in λ increases g_m and a decrease in α decreases g_m.[30] I explore below whether the model's predictions about the

[29] Note that $g_\ell < 0$ since $\delta < 1$.

[30] If the changes in α and λ were unanticipated by Intel, the formula derived in the paper for g_m can be used to compare growth across phases. The formula is based on the policies that Intel would follow, given the values of α and λ. Since these changes were unanticipated, Intel would select policies assuming the current values of λ and α to continue forever. There is anecdotal evidence to suggest that changes in λ and α were unanticipated. That the change in λ was unanticipated can be seen from 'The International Technology Roadmap for Semiconductors,' a consensus document drawn up every two years by representatives from leading semiconductor companies, which projects a timeline for the values of the different parameters in the industry for the next 15 years (see, for example, ITRS [2001]). In versions of the Roadmap in the 1990's, the forecasts assumed new capital equipment with smaller ℓ to arrive every three years. The versions of the Roadmap in the early 2000's noted that new capital equipment had in fact arrived every two years on average in the 1990s. Gelas [2005] recounts

response of other variables to unanticipated changes in λ and α are consistent with the data.

The changes in λ do not affect the static policies—$T^*(\ell)$, $m^*(\ell)$, $y^*(\ell)$, c^* or p^*, as can be seen from equations (4)–(10). Such changes do affect the threshold lag x^* in equation (14) and possibly the optimal adoption policy, n^*. To characterize the changes in n^* induced by changes in λ, I use the fact that any change in n^* would affect the present discounted value of the firm. Let $\bar{V}(n, \lambda)$ be the present discounted value of the firm if it adopts every n^{th} innovation, given an arrival rate λ. Clearly, the optimal adoption policy n^* should satisfy

$$n^* = \arg\max_n \bar{V}(n, \lambda).$$

Proposition 3 derives the function $\bar{V}(n, \lambda)$.

Proposition 3. Given the innovation rate λ, the expected present discounted value of adopting every n^{th} innovation is

$$\bar{V}(n,\lambda) = \frac{1}{\bar{\ell}_0^{\varphi}}\left[\frac{\left\{1-\left(\frac{\lambda}{\rho+\lambda}\right)^n\right\}\frac{\pi}{\rho}-\left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^n F(1)}{1-\left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^n}\right]$$

See Appendix for proof.

I evaluate the expression $\bar{V}(n, \lambda)$ for plausible parameter values of $\{\delta, F(1), \pi, \rho, \varphi, \bar{\ell}_0\}$ for different values of λ and n[31]. Figure 7 shows the result of a sample simulation for $n = \{3, 4, 5\}$.

As can be seen from the figure, n^* is weakly increasing with λ, the intuition for which is provided by the value matching condition in equation (15). An increase in λ increases the value of waiting, the right hand side of equation (15), since the probability of an innovation's arriving the next instant in time is higher. Hence the firm might find it optimal to wait for more innovations to arrive before adopting. The optimal value n^* actually increases only if the increase in λ is sufficiently high. The model thus allows

anecdotal evidence that the change in α was unanticipated by Intel. Intel introduced the Pentium chip in 1993 and since then has made extensions of the Pentium design in the form of Pentium II, Pentium III and Pentium 4. But in the early 2000's, new microprocessors introduced with the Pentium 4 design, encountered many engineering difficulties. Intel gave up on pursuing further extensions of the Pentium 4, and adopted a new design based on a multicore structure. As recounted in the article, Intel had announced plans to push the extensions of the Pentium 4 microprocessors for many years to come, indicating that the problems that they encountered were unanticipated.

[31] The parameter values used are $\delta = 0.9$, $F(1) = 1.3$, $\pi = 5$, $\rho = 0.25$, $\varphi = 0.86$, $\bar{\ell}_0 = 1$.

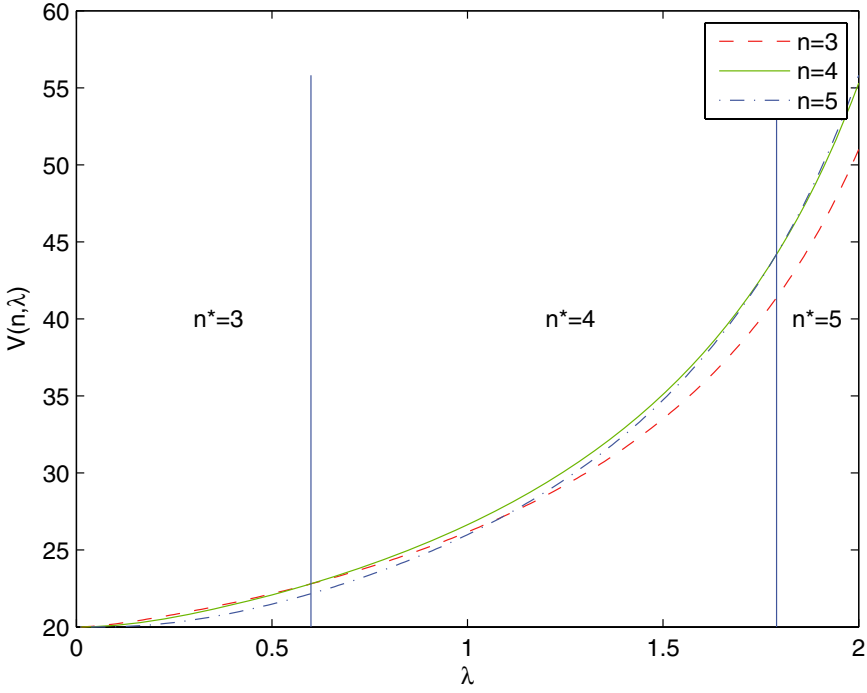

Figure 7
Variation of n^* with λ

Notes: The y-axis variable, $\bar{V}(n,\lambda)$ is the present discounted value of the firm if it adopts every n^{th} innovation, given arrival rate λ. The optimal adoption policy n^* is the value of n that maximizes $\bar{V}(n,\lambda)$. As can be seen from the graph, n^* is weakly increasing in λ.

for the possibility that an increase in λ could occur without inducing any change in the adoption policy n^*. If there were an increase in n^* going from Phase I to Phase II then the scaling factor, δ^{n^*}, should have decreased. The average scaling factor has not decreased going from Phase I to Phase II, as can be seen from Figure 3. The possibility that in going from Phase I to Phase II, there were an increase in λ without a change in n^*, finds further support in the data on the time interval between adoptions. Since the adoption interval, $\Delta\tau_j \equiv \tau_j - \tau_{j-1}$, is the time taken for n^* Poisson events to happen, it follows that $\Delta\tau_j \sim \mathbf{G}\left(n^*, \frac{1}{\lambda}\right)$, where $\mathbf{G}$ is the gamma distribution. The mean adoption interval is then the mean of $\mathbf{G}\left(n^*, \frac{1}{\lambda}\right)$, which is equal to $\frac{n^*}{\lambda}$. If there were an increase in λ without a change in n^*, then the mean adoption interval, $\frac{n^*}{\lambda}$, should have decreased. The average adoption interval did in fact decrease from 4.35 years in Phase I to 2.10 years in Phase II (this is easily seen in Figure 2).

A change in α affects the static optimal policies. A decrease in α does not change the elasticity of $T^*(\ell)$ (which still remains at 2) but decreases the

TABLE III
ESTIMATES OF φ FROM THE REVENUE FUNCTION AND GROSS PROFIT FUNCTION

	Phase II	Phase III
Using $r^*(\ell)$	–0.97	–0.26
	(0.098)	(0.12)
Using $\pi^*(\ell)$	–0.99	–0.28
	(0.07)	(0.19)

Notes: The first row shows φ estimated from the equation $\ln(r^*) = constant + \varphi \ln(\ell)$. The data for revenues were taken from Intel's annual reports. The average annual revenue over the years of operation of a vintage ℓ is taken as $r^*(\ell)$. The years of operation of a vintage ℓ is taken to be the years between the year in which ℓ was adopted to the year the next vintage was adopted. The second row shows the estimate for φ obtained with a similar approach using the gross profit function $\pi^*(\ell)$.

elasticity of the $m^*(\ell)$ which is given by $(1 + 2\alpha)$.[32] Indeed, this paper argues that a decrease in the elasticity of $m^*(\ell)$ caused the slowdown in growth of m, and is evident in the data (see Table IV). A decrease in α would also reduce the optimal marginal cost c^* and price p^*. Further, it would reduce the elasticity of the revenue function $r^*(\ell)$ and gross profit function $\pi^*(\ell)$, both given by $\varphi = (1 + 2\alpha)(\eta - 1)$ (see equations (11) and (12)). The lack of data on prices, marginal costs and quantity sold for the whole time span studied in this paper, makes it difficult to check the predictions of the model against the data for these variables.[33] However revenues and gross profits of Intel are available from Intel's annual reports.[34] Table III reports the value of φ estimated using the data from annual reports. The elasticity φ decreased from 0.97 in Phase II to 0.26 in Phase III when estimated from the revenue function $r^*(\ell)$, and from 0.99 to 0.28 when estimated from the gross profit function $\pi^*(\ell)$, consistent with the hypothesis that there was a decrease in α in going from Phase II to Phase III. A change in α would also change π (see equation (8)) and hence the threshold lag x^* (see equation 14) and possibly the choice of adoption policy n^* and the scaling factor δ^{n^*}. Similar to the analysis for an unanticipated change in λ above, unless the change in α is sufficiently large, it will not lead to a change in n^*. As can be

[32] Note that in referring to elasticity, I take absolute values, for example the elasticity of $m^*(\ell)$ is $\left|\frac{\partial m^*(\ell)}{\partial \ell} \Big/ \frac{m^*(\ell)}{\ell}\right|$.

[33] According to equation (10), a drop in α from 0.78 to 0.14 (the values estimated for Phase II and Phase III respectively, as shown in Table IV) should lead to a 47% reduction in prices. The price data for microprocessors for the years 1993–2004 is available from MicroDesign Resources. The average price for the period 1993–2000 is 300.36 and the average price during 2001–2004 is 228.86. This implies a price drop of 31%, which is less than the 47% predicted by the model. However, including the price data from years 2005–2008 would probably reduce the price in Phase III to less than 228.86, and reduce the actual drop in price to more than 31%. Hence, the drop in α accounts for most of the drop in price seen in the data.

[34] During the Phase II and Phase III years, most of Intel's revenues and profits came from sales of microprocessors, and hence the revenues and gross profits reported in annual reports can be taken to be a very close approximation of the revenues and profits from microprocessor sales.

seen from Figure 3, the scaling factor δ^{n^*} has not changed between Phases II and III, suggesting again that n^* did not change. If neither n^* nor λ changed in going from Phase II to Phase III, then the model predicts that the mean adoption interval $\frac{n^*}{\lambda}$ should not have changed either. This prediction is borne out in the data: the mean adoption interval was 2.03 years in Phase II, quite close to the 2.10 years in Phase III. Thus, the changes seen in the data are consistent with what the model predicts should have been the response of Intel to an unanticipated increase in λ in Phase I and an unanticipated decrease in α in Phase II.

There are two alternative explanations for the change in the rate of technological progress which I examine below. The first candidate is that the acceleration in Phase II was caused by a positive demand shock for microprocessors resulting from the Internet technology boom of the 1990's and the ensuing slowdown in Phase III was caused by the negative demand shock resulting from the collapse of many technology companies in early 2000's. As shown by equations (8) and (12), a change in D (a positive or negative demand shock) would lead to a change in profit from any vintage. If the change in profit is sufficiently large, it can in turn affect the adoption policy n^* (equation (15)) and hence the frequency of new vintage adoptions. But this would also affect δ^{n^*}, the factor by which ℓ scales at each adoption. However, as noted in stylized fact (1), the scaling factor has remained roughly constant across the three phases.[35] Further, a positive demand shock can lead to more frequent adoptions with smaller sized technological improvements at each adoption (and a negative demand shock can lead to less frequent adoptions with larger sized technological improvements at each adoption) but the average growth rate of performance should remain the same as before (see equation (16)). There was accelerated growth in the industry for a period of ten years (the duration of Phase II) and slowdown for over at least eight years, relatively long periods given the pace of growth in the industry. Hence one would like to look for an explanation that allows for a change in the average growth rate of performance.

The second candidate explanation for the acceleration and slowdown is that there were changes in the rate of learning-by-doing in the industry, across the three phases. Learning by doing in the semiconductor industry is primarily within a vintage and arises from improvements in production yield over time (see Krugman and Baldwin [1986] and Irwin and Klenow [1994]), as a firm learns to use the new vintage of capital equipment. While learning by doing contributes to the decline in manufacturing cost of a given microprocessor over its lifetime, it does not play an important role in the declines in cost per quality unit of microprocessors over long periods of

[35] The average values of the scaling factor was 0.6, 0.7 and 0.7 in Phases I, II and III respectively.

time. Such declines result from increases in quality (performance) over time because of the adoption of new vintages of capital equipment, with the average cost of microprocessors over their lifetimes remaining roughly constant. Aizcorbe [2006] finds that average cost per microprocessor computed over its lifetime (which corresponds to $\bar{c}$ in the paper), increased slightly (by 3.7%) during 1993–1999, and she concludes that reduction in cost per microprocessor through learning could not have been a driver of the acceleration.

In the next section, I quantitatively assess the contributions of changes in λ and α to the acceleration and slowdown.

V(i). *Decomposition of Changes in Growth of Performance*

For two time periods t and t', equation (16) implies that

$$\frac{g_{m_{t'}}}{g_{m_t}} = \left(\frac{\lambda_{t'}}{\lambda_t}\right)\left(\frac{1+2\alpha_{t'}}{1+2\alpha_t}\right). \tag{17}$$

since δ is assumed to be the same across all periods. A change in the rate of technological progress, $\frac{g_{m_{t'}}}{g_{m_t}}$, can thus be neatly separated into contributions from the semiconductor equipment sector, $\frac{\lambda_{t'}}{\lambda_t}$, and from Intel, $\frac{1+2\alpha_{t'}}{1+2\alpha_t}$. The estimates of α and λ for the three periods, in conjunction with equation (17), can be used to quantitatively decompose the changes in g_m. I estimate the value of λ for the three periods using data on adoption intervals, $\Delta\tau_j$. Since $\Delta\tau_j \sim \mathbf{G}\left(n^*, \frac{1}{\lambda}\right)$, the parameters n^* and λ can be estimated by the maximum likelihood method using the data on $\Delta\tau_j$. There are, however, only 13 data points for $\Delta\tau_j$, since Intel has made just 14 adoptions in the period 1971–2008. Hence the sample for each phase considered separately is very small. Fortunately, the model provides a useful guideline to aid the estimation. The data on the scaling factor implies that n^* has remained constant across the three phases (see stylized fact 1 and Figure 3). Hence I estimate n^* using the data on $\Delta\tau_j$ pooled together from all three phases and use this value of n^* to estimate λ for the three phases separately. The maximum likelihood estimates of λ and n^* can be estimated using the result in Proposition 4).

Proposition 4. Let $\{\Delta\tau_j\}_{j=1}^{J}$ be an *i.i.d* sample from $\mathbf{G}\left(n^*, \frac{1}{\lambda}\right)$, with sample mean $\Delta\bar{\tau}$. Then the maximum likelihood estimates $\left(\hat{n}^*, \hat{\lambda}\right)$ satisfies $\hat{\lambda} = \frac{\hat{n}^*}{\Delta\bar{\tau}}$.

See Appendix for proof.

Hence the MLE estimates can be calculated by a simple procedure. For every positive integer n^*, find the optimal λ using the condition above. Then choose the (λ, n^*) pair that maximizes the likelihood function. Using the data on Intel's adoption intervals, this procedure gives maximum likelihood estimates of $n^* = 4$, $\lambda_1 = 0.92$, $\lambda_2 = 1.96$ and $\lambda_3 = 1.90$, where λ_1, λ_2 and

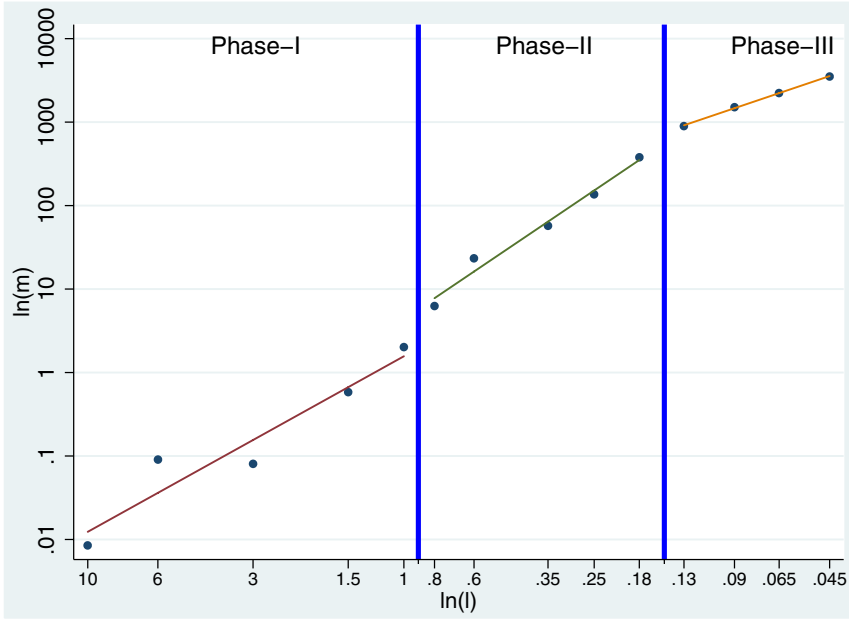

Figure 8
Strong Relationship between Performance (m) and Vintage (ℓ) in each Phase
Notes: The performance a vintage is taken to be average the performances of all microprocessors manufactured with that vintage.

λ_3 are the innovation rates in Phase I, Phase II and Phase III respectively.[36] The bootstrap distribution of the estimates of n^* and λ are given in Figure 9.

For estimating α, equation (6) implies that α can be obtained from the regression, $\ln(m) = constant + (1 + 2\alpha)\ln(\ell)$.[37] The estimates of λ and α are given in Table IV. As can be seen from the table, α dropped in Phase III.

The decomposition of the acceleration and slowdown into contributions from the two sectors, using the estimated values of λ and α, is shown in Table V. Note that a contribution of 1 means that the corresponding sector did not play a role in the acceleration or slowdown. It can be seen from the first row that g_m increased by a factor of 1.79 going from Phase I to II . The

[36] A larger dataset of all innovations (including those not adopted by Intel) produced by the equipment firms would have allowed the use of other methods to estimate λ independently of the estimate of n^*. Such a dataset is however not available. While the data on some unadopted innovations are available from the website of equipment companies (as shown in Figure 6), this list is not exhaustive. Moreover, the websites and online articles do not usually contain the dates at which equipment was first available in the market.

[37] Note that *constant* in the regression corresponds to $\ln(m_0\alpha^\alpha)$ (see equation (6). The regression is done separately for each phase and I assume α to be constant in each phase.

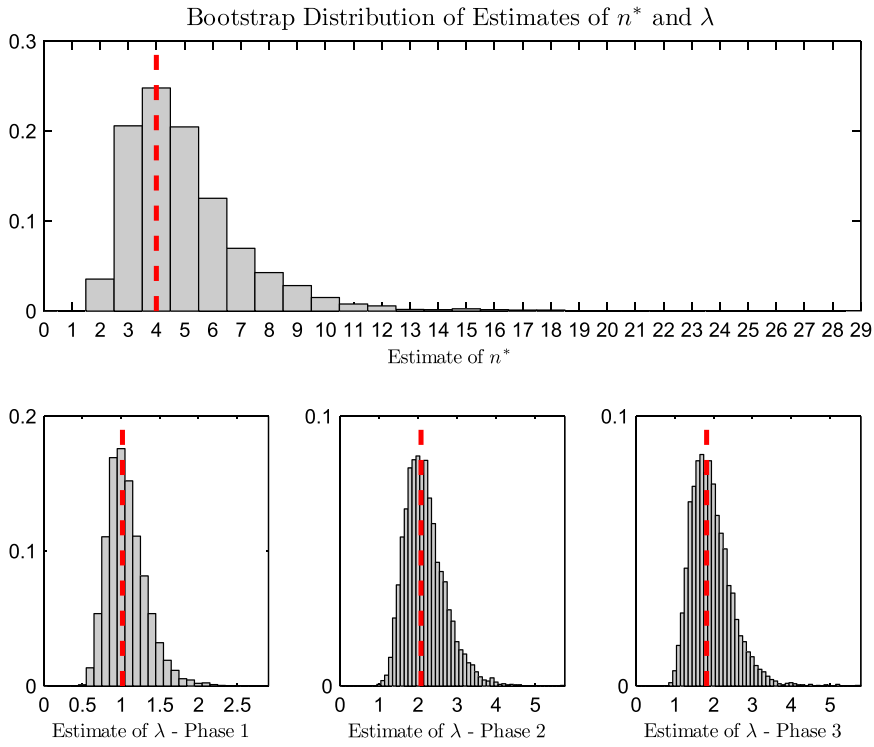

Figure 9
Bootstrap Distribution

Notes: For obtaining the distribution for n^*, 5,000 random samples (with size of the observed sample) were drawn from a gamma distribution with parameters that were the MLE estimates obtained from the observed sample. The MLE estimate of n^* was calculated for each random sample to obtain the above distribution. The MLE estimate of n^* from the observed sample was used to calculate the estimate of λ for each phase. For obtaining the distribution of λ's for each phase, random samples (with size corresponding to the number of observations in each phase) were drawn from a gamma distribution with the parameters equal to the estimated parameters. The MLE estimate for λ was calculated for each sample, assuming the n^* to be the value estimated from the observed sample. The resulting distribution of λ's are shown above. The x-axis values of the vertical dashed lines in the graphs correspond to the estimated parameter values.

TABLE IV
ESTIMATES OF α

	Phase 1	Phase II	Phase III
α	0.53	0.78	0.14
	(0.18)	(0.10)	(0.02)

Notes: The parameter α is estimated from the regression $\ln(m) = constant + (1 + 2\alpha)\ln(\ell)$. A plot of $ln(m)$ against $ln(\ell)$ is shown in Figure 8.

TABLE V
DECOMPOSITION OF THE ACCELERATION AND SLOWDOWN

	Change in Rate of Technological Progress $\frac{g_{m_{t'}}}{g_{m_t}}$	Contribution of Equipment. Co. $\frac{\lambda_{t'}}{\lambda_t}$	Contribution of Intel $\frac{1+2\alpha_{t'}}{1+2\alpha_t}$
Acceleration	1.79	2.13	1.24
Slowdown	0.46	0.97	0.50

Notes: Equation (16) stipulates that the entries in the second column should equal the product of the entries in the third and fourth columns. A value of 1 for the third or fourth column means that the corresponding sector did not play any role in the change in g_m. As can be seen from the entries in the second row, the equipment firms played the important role in the acceleration; the role played by Intel was minimal. For the slowdown, on the other hand, Intel was responsible and the equipment companies hardly contributed.

contribution from semiconductor equipment industry increased by a factor of 2.13 and the contribution from Intel increased by factor of 1.24. Hence, the increase in g_m was caused overwhelmingly by an increase in the innovation rate in the semiconductor equipment industry λ, and very little was accountable to improvements in Intel's own efficiency α.[38] The slowdown, however, was caused entirely by a decrease in Intel's own efficiency α, as can be seen from the second row of Table V.

The finding that there was an increase in the innovation rate λ in the semiconductor equipment industry after Phase I has been corroborated in other studies, including Jorgenson [2001] and Aizcorbe, Oliner and Sichel [2008], who report it in terms of decrease in the time interval between the adoption of new vintages. A possible explanation for the increase in λ, suggested in Hutcheson [2005], is that it was the outcome of R&D coordination activities in the semiconductor equipment industry undertaken by SEMATECH, an industrial research consortium established in 1988.[39] It

[38] The two contributions taken together account for more than the 1.79 factor increase in performance seen in the data, and this discrepancy must be taken to be the result of factors not taken into consideration in this model. One possible explanation for this is that the first adopters of semiconductor equipment during Phase I were DRAM (memory chip) producers and not microprocessor producers. In the later years, microprocessor firms adopted at the same time, if not earlier, than DRAM producers. The presence of possible adoption lags during Phase I would mean that the actual innovation rate λ_1 is lower than the estimated value, which might account for the discrepancy above.

[39] Faced with continuing loss of market share to Japanese companies, in 1988 leading U.S. semiconductor companies formed a research consortium, SEMATECH, with the help of an annual subsidy from the U.S. government. SEMATECH started issuing biennial Technology Roadmaps stating the technological barriers to be overcome to create the next vintage of semiconductor equipment, and the possible solutions to overcome these barriers. The roadmaps proved to be a tremendous success in the industry, and turned out to be a point of coordination among the different firms in the industry. This success led SEMATECH gave up its national focus and it became International SEMATECH, and the roadmap was renamed the 'International Technology Roadmap for Semiconductors' (ITRS). SEMATECH continues to the be a central point for coordinating R&D in semiconductor equipment, and the biannual release of the 'International Technology Roadmap for Semiconductors' is continuing to this day. Flamm [2010] contains an excellent summary of the evolution of

remains a topic of further research to understand the cause of the increase in the innovation rate, and to examine the possible role played by SEMATECH. On the other hand, there is widespread agreement in the semiconductor industry on the reason for the drop in efficiency α, which caused the slowdown. As mentioned in section I, in the early 2000's, microprocessors with new designs introduced by Intel hit a well publicized problem, the microprocessors generated a large amount of heat during their operation which affected their proper functioning. Since then Intel has abandoned the pattern of design improvements that it had followed in the past and adopted a new approach, the multicore design. The multicore approach is less effective than previous approaches in translating increases in the number of transistors available on a chip to increases in performance. The inability of Intel's designs to get the most out of the new transistors is captured in the model as a drop in the efficiency α.

Finally, it should be noted that although the explanations for the acceleration and slowdown suggested here are based on shifts in model parameters, there are key relationships in the model that have not changed across the three phases. The scaling factor has remained roughly constant across the three phases (see Figure 3). Similarly, the relationship between T and ℓ has not changed across the three phases (see Figure 4).

VI. CONCLUSION

This paper develops an economic model of the microprocessor industry that endogenizes technological progress in the industry. The model captures well the evolution of different engineering and economic variables in the industry and connects the engineering and economic measures of technological progress. The model was used to understand the cause of the acceleration in technological progress in the industry during 1990–2000 and the subsequent slowdown. Three conclusions emerge from this application of the model. First, the acceleration in technological progress was driven by an increase in the innovation rate in the upstream semiconductor equipment industry leading to more rapid adoption of innovations by Intel. Second, the slowdown was caused by a decrease in the efficiency with which Intel was able to use the innovations generated by the semiconductor equipment industry. Third, innovation in the semiconductor equipment industry has been the main workhorse driving technological progress in the microprocessor industry since 2001. However, further innovation in the semiconductor equipment industry is becoming ever more difficult as the

SEMATECH, its role in coordinating R&D efforts across semiconductor companies through the road-mapping process, and its impact on innovation in the semiconductor equipment industry.

industry approaches the physical limit to reducing the size of the transistor. If innovations in the semiconductor equipment industry slow down, then it will accentuate the existing difficulties in maintaining the rate of technological progress in the microprocessor industry.

APPENDIX

Proofs of Propositions

Proof of Proposition 1. Equation (13) can be rewritten as

$$v(x) = \frac{\pi}{\rho + \lambda} x^{\varphi} + \frac{1}{\delta^{\varphi}} \frac{\lambda}{\rho + \lambda} [Max\{v(\delta x), v(1) - F(1)\}]$$

where $x \in (0, 1]$. Consider the operator T, that maps functions defined on (0, 1] as

$$T(f(x)) = \frac{\pi}{\rho + \lambda} x^{\varphi} + \frac{1}{\delta^{\varphi}} \frac{\lambda}{\rho + \lambda} [Max\{f(\delta x), f(1) - F(1)\}]$$

$T(.)$ maps continuous functions to continuous functions. Moreover, it is easily seen from the conditions in Blackwell [1965] that T is a contraction mapping. Hence by the contraction mapping theorem there exists a unique $v(x)$ that solves the Bellman equation above. Moreover, T maps weakly increasing functions to strictly increasing functions, hence $v(x)$ is strictly increasing (see Stokey, Lucas and Prescott [1989]). Hence, there exists a value x^* such that

$$v(x^*) = v(1) - F(1). \tag{18}$$

Moreover, since $v(.)$ is an increasing function and $\delta < 1$

$$v(\delta x^*) < v(1) - F(1). \tag{19}$$

Evaluating the Bellman equation (VI) at $x = x^*$ and using equations (18) and 19 gives,

$$v(x^*) = \frac{\pi}{(\rho + \lambda)} x^{*\varphi} + \frac{1}{\delta^{\varphi}} \frac{\lambda}{(\rho + \lambda)} Max\{v(\delta x^*), [v(1) - F(1)]\}$$

$$v(1) - F(1) = \frac{\pi}{(\rho + \lambda)} x^{*\varphi} + \frac{1}{\delta^{\varphi}} \frac{\lambda}{\rho + \lambda} [v(1) - F(1)]$$

which gives

$$x^* = \left\{ \left(\rho + \lambda - \frac{\lambda}{\delta^{\varphi}} \right) \left(\frac{v(1) - F(1)}{\pi} \right) \right\}^{\frac{1}{\varphi}} \qquad \square$$

Proof of Proposition 2. Let ℓ_0 be the value of ℓ at time t and let ℓ' be the random variable representing the value of ℓ after time interval Δt. The mean growth rate of ℓ is,

$$g_\ell = \lim_{\Delta t \to 0} \frac{E(\ln(\ell')) - \ln(\ell_0)}{\Delta t} \tag{20}$$

Denote by n the random variable representing the number of innovations that arrive in time interval Δt, and denote by m the random variable representing the number of adoptions that the firm makes in time interval Δt. Since the firm adopts every n^*th innovation, m is the greatest integer less than $\frac{n}{n^*}$, i.e.,

$$m = \left[\frac{n}{n^*}\right], \tag{21}$$

Therefore, $\ell' = \left(\delta^{n^*}\right)^m \ell_0$, and

$$E(\ln(\ell')) = E\left(m \ln\left(\delta^{n^*}\right) + \ln(\ell_0)\right) = \ln\left(\delta^{n^*}\right) E(m) + \ln(\ell_0). \tag{22}$$

From equation (21),

$$E(m) = E\left(\left[\frac{n}{n^*}\right]\right) = \frac{E(n)}{n^*} = \frac{\lambda \Delta t}{n^*}, \tag{23}$$

where the last step follows from the fact that the expected number of arrivals in time interval Δt for a Poisson process with rate parameter λ is $\lambda \Delta t$. Substituting equation (23) in equation (22) gives,

$$E(\ln(\ell')) = n^* \ln(\delta) \frac{\lambda \Delta t}{n^*} + \ln \ell_0 = \lambda \Delta t \ln(\delta) + \ln \ell_0.$$

Hence equation (20) implies,

$$g_\ell = \lim_{\Delta t \to 0} \frac{\lambda \Delta t \ln(\delta) + \ln(\ell_0) - \ln(\ell_0)}{\Delta t} = \lambda \ln(\delta) \qquad \square$$

Proof of Proposition 3. Let $\{\Delta \tau_j\}_{j=0}^{\infty}$ be the adoption intervals. Then the ith adoption with vintage $\ell_i = \left(\delta^n\right)^i \bar{\ell}_0$, occurs at time $\tau_i = \sum_{j=0}^{i-1} \Delta \tau_j$. Then if the firm follows the policy of adopting every nth innovation, the net profit of the firm in the ith adoption interval (i.e., the profit from operating the ith vintage equipment), discounted back to $t = 0$ is, $\Pi_i(n, \lambda) =$

$$e^{-\rho \tau_i} \left\{ \int_0^{\Delta \tau_i} e^{-\rho t} \frac{\pi}{\left(\delta^{ni} \bar{\ell}_0\right)^\varphi} dt - \frac{F(1)}{\left(\delta^{ni} \bar{\ell}_0\right)^\varphi} \right\} = e^{-\rho \sum_{k=0}^{i-1} \Delta \tau_k} \frac{1}{\delta^{ni\varphi} \bar{\ell}_0} \left\{ \frac{\pi}{\rho} \left(1 - e^{-\rho \Delta \tau_i}\right) - F(1) \right\}$$

Then the present discounted value of net profits obtained under the policy of adopting every n^{th} innovation is $\sum_{i=0}^{\infty}\Pi_i(n,\lambda)$, which is given by $\sum_{i=0}^{\infty}\Pi_i(n,\lambda) =$

$$\frac{1}{\ell_0^{\varphi}}\left[\sum_{i=0}^{\infty}\frac{1}{\delta^{ni\varphi}}e^{-\rho\sum_{k=0}^{i-1}\Delta\tau_k}\frac{\pi}{\rho}-\sum_{i=1}^{\infty}\frac{1}{\delta^{ni\varphi}}e^{-\rho\sum_{k=0}^{i-1}\Delta\tau_k}F(1)-\sum_{i=0}^{\infty}\frac{1}{\delta^{ni\varphi}}e^{-\rho\sum_{k=0}^{i}\Delta\tau_k}\left(\frac{\pi}{\rho}\right)\right]$$

Then
$$\begin{aligned}\bar{V}(n,\lambda) &= E\sum_{i=0}^{\infty}\Pi_i(n,\lambda)\\ &= \frac{1}{\ell_0^{\varphi}}\left[\sum_{i=0}^{\infty}\frac{1}{\delta^{n^*i\varphi}}\frac{\pi}{\rho}E\left[e^{-\rho\sum_{k=0}^{i-1}\Delta\tau_k}\right]-\sum_{i=1}^{\infty}\frac{1}{\delta^{n^*i\varphi}}F(1)E\left[e^{-\rho\sum_{k=0}^{i-1}\Delta\tau_k}\right]\right.\\ &\quad\left.-\sum_{i=0}^{\infty}\frac{1}{\delta^{n^*i\varphi}}\left(\frac{\pi}{\rho}\right)E\left[e^{-\rho\sum_{k=0}^{i}\Delta\tau_k}\right]\right]\end{aligned}$$

The adoption interval $\Delta\tau_j$ is the time taken for n^* Poisson events to happen. Hence $\Delta\tau_j$ are independent draws from the Gamma distribution $\mathbf{G}\left(n^*,\frac{1}{\lambda}\right)$. It follows that $\sum_{j=0}^{i-1}\Delta\tau_j \sim \mathbf{G}\left(n^*i,\frac{1}{\lambda}\right)$. To evaluate the above expectations, I use Proposition 5, which shows that $E\left[e^{-\rho\Delta\tau_i}\right]=\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*}$. This implies

$$\begin{aligned}\bar{V}(n,\lambda) &= E\sum_{i=0}^{\infty}\Pi_i(n,\lambda)\\ &= \frac{1}{\ell_0^{\varphi}}\left[\sum_{i=0}^{\infty}\frac{1}{\delta^{n^*i\varphi}}\frac{\pi}{\rho}\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*i}-\sum_{i=1}^{\infty}\frac{1}{\delta^{n^*i\varphi}}F(1)\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*i}-\sum_{i=0}^{\infty}\frac{1}{\delta^{n^*i\varphi}}\left(\frac{\pi}{\rho}\right)\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*(i+1)}\right]\end{aligned}$$

Evaluating the sums of geometric series, the above expression reduces to

$$\bar{V}(n,\lambda)=E\sum_{i=0}^{\infty}\Pi_i(n,\lambda)=\frac{1}{\ell_0^{\varphi}}\left[\frac{\left\{1-\left(\frac{\lambda}{\rho+\lambda}\right)^{n}\right\}\frac{\pi}{\rho}-\left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^{n}F(1)}{1-\left(\frac{1}{\delta^{\varphi}}\frac{\lambda}{\rho+\lambda}\right)^{n}}\right] \qquad \square$$

Lemma 5. If $\Delta\tau_i \sim \mathbf{G}\left(n^*,\frac{1}{\lambda}\right)$, then $E\left[e^{-\rho\Delta\tau_i}\right]=\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*}$

Proof of Lemma 5. Since $G\left(n^*,\frac{1}{\lambda}\right)=\frac{\lambda^{n^*}\Delta\tau_j^{n^*-1}e^{-\lambda\Delta\tau_j}}{\Gamma(n^*)}$, where $\Gamma(n^*)=(n-1)!$ is the Gamma function,

$$E\left[e^{-\rho\Delta\tau_i}\right]=\int_0^\infty e^{-\rho t}\frac{\lambda^{n^*}\Delta\tau^{n^*-1}e^{-\lambda T}}{\Gamma(n^*)}d\Delta\tau=\frac{\lambda^{n^*}}{\Gamma(n^*)}\frac{n^*-1}{\rho+\lambda}\int_0^\infty \Delta\tau^{n^*-2}e^{-(\rho+\lambda)\Delta\tau}d\Delta\tau$$
$$=\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*}\frac{(n^*-1)!}{\Gamma(n^*)}=\left(\frac{\lambda}{\rho+\lambda}\right)^{n^*}$$

Proof of Proposition 4. Using the p.d.f for gamma distribution, the probability that these J observations are drawn from $\mathbf{G}\left(n^*, \frac{1}{\lambda}\right)$ is

$$\prod_{j=1}^{J}\frac{\lambda^{n^*}\Delta\tau_j^{n^*-1}e^{-\lambda\Delta\tau_j}}{\Gamma(n^*)}$$

where $\Gamma(n^*)=(n^*-1)!$ is the gamma function. The log-likelihood function is then

$$L(n^*,\lambda)=\sum_{j=1}^{J}\left\{-\ln[\Gamma(n^*)]+n^*\ln(\lambda)+(n^*-1)\ln\left(\Delta\tau_j\right)-\lambda\Delta\tau_j\right\}$$
$$=-J\ln[\Gamma(n^*)]+Jn^*\ln(\lambda)+(n^*-1)\sum_{j=1}^{J}\ln\left(\Delta\tau_j\right)-\lambda\sum_{j=1}^{J}\Delta\tau_j$$

Let $(\hat{n}^*,\hat{\lambda})$ be the maximum likelihood estimate. Then $\frac{\partial L}{\partial\lambda}\left(\hat{n}^*,\hat{\lambda}\right)=0$, which gives $\frac{J\hat{n}^*}{\hat{\lambda}}-\sum_{j=1}^{J}\Delta\tau_j=0$ and hence $\hat{\lambda}=\frac{J\hat{n}^*}{\sum_{j=1}^{J}\Delta\tau_j}=\frac{\hat{n}^*}{\Delta\bar{\tau}}$.

Data Sources

The dataset contains the following characteristics for every microprocessor made by Intel since the first microprocessor in 1971—product name, date of release, performance (m), vintage (ℓ), transistors (T). There are a total of 588 microprocessors for Intel. Among these, 135 microprocessors are in the low value category, which Intel sells under the name Celeron. These are usually defective parts which are sold at a low price. Hence I omit these microprocessors in this paper. This leaves a total of 453 microprocessors for Intel. The server processors manufactured by Intel have also been left out since functionally they are very different from desktop and laptop microprocessors, which form the focus of this paper. The data for m was obtained from two sources—Standard Performance Evaluation Corporation (SPEC) and Business Applications Performance Corporation (BAPCo). SPEC and BAPCO are industry consortia of which both microprocessor producers, Intel and AMD, are members. The data for T and ℓ were obtained from The Intel website and confirmed against other online reports and articles.

REFERENCES

Aizcorbe, A., 2005, 'Moore's Law, Competition and Intel's Productivity in the Mid-1990's,' *American Economic Review*, 95, pp. 305–308.

Aizcorbe, A., 2006, 'Why Did Semiconductor Price Indexes Fall So Fast in the 1990's? A Decomposition,' *Economic Inquiry*, 44, pp. 485–496.

Aizcorbe, A. and Kortum, S., 2005, 'Moore's Law and the Semiconductor Industry: A Vintage Model,' *Scandinavian Journal of Economics*, 107, pp. 603–630.
Aizcorbe, A.; Oliner, S. D. and Sichel, D. E., 2008, 'Shifting Trends in Semiconductor Prices and the Pace of Technological Progress,' *Business Economics*, 43, pp. 23–29, Palgrave Macmillan.
Balcer, Y. and Lippman, S. A., 1984, 'Technological Expectations and Adoption of Improved Technology,' *Journal of Economic Theory*, 34, pp. 292–318.
Baldwin, R. and Krugman, P., 1986, 'Market Access and International Competition: A Simulation Study of 16K Random Access Memories,' working paper, NBER. (National Bureau of Econmic Research, Cambridge, Massachusetts, U.S.A.)
Berglund, C. N., 1996, 'A Unified Yield Model Incorporating Both Defect and Parametric Effects,' *IEEE Transactions on Semiconductor Manufacturing*, 9, pp. 447–454.
Blackwell, D., 1965, 'Discounted Dynamic Programming,' *Annals of Mathematical Statistics*, 36, pp. 226–235.
Borkar, S., 1999, 'Design Challenges of Technology Scaling,' *IEEE Micro*, 19, pp. 23–29.
Borkar, S. and Chien, A., 2011, 'The Future of Microprocessors,' *Communications of the ACM*, 54, 67–77.
Condon, S., 2009, 'Intel to Invest $7 Billion in U.S. Manufacturing Facilities CNET, *http://news.cnet.com/8301-13578 3-10160368-38.html*.
Dixit, A. K. and Pindyck, R. S., 1994, *Investment under Uncertainty* (Princeton University Press, Pinceton New Jersey, U.S.A.).
Farzin, Y. H.; Huisman, K. J. M. and Kort, P. M., 1998, 'Optimal Timing of Technology Adoption,' *Journal of Economic Dynamics and Control*, 22, pp. 779–799.
Flamm, K., 2004, 'Moore's Law and the Economics of Semiconductor Price Trends,' in D. W. Jorgenson and C. W. Wessner (eds), *Semiconductors: Trends, Implications, and Questions Report of a Symposium*, pp. 151–170. (National Academies Press, 500 Fifth Street N.W., Washington, D.C., U.S.A.).
Flamm, K., 2010, 'Economic Impacts of International R&D Coordination: SEMATECH and the International Technology Roadmap,' in Nagaoka S., Kondo M., Flamm K. and Wessner C. (eds), *21st century Innovation Systems for Japan and the United States: Lessons from a Decade of Change*, pp. 108–125. (National Academies Press, 500 Fifth Street N.W., Washington, D.C., U.S.A.).
Gelas, J. D., 2005, 'The Quest for More Processing Power, Part One: Is the Single Core CPU Doomed?,' *http://www.anandtech.com/show/1611*.
Goettler, R. L. and Gordon, B. R., 2011, 'Does AMD Spur Intel to Innovate More?,' *Journal of Political Economy*, 119, pp. 1141–1200.
Gordon, B. R., 2009, 'A Dynamic Model of Consumer Replacement Cycles in the PC Processor Industry,' *Marketing Science*, 28, pp. 846–867.
Gordon, R. J., 2002, 'Technology and Economic Performance in the American Economy,' NBER working paper 8771, (National Bureau of Economic Research).
Griliches, Z., 1957, 'Hybrid Corn: An Exploration in the Economics of Technological Change,' *Econometrica*, 25, pp. 501–522.
Grimm, B., 1998, 'Price Indexes for Selected Semiconductors, 1974–96,' *Survey of Current Business*, pp. 824.
Hoppe, H. C., 2002, 'The Timing of New Technology Adoption: Theoretical Models and Empirical Evidence,' *Manchester School*, 70, pp. 56–76.
Hulten, C. R., 1978, 'Growth Accounting with Intermediate Inputs,' *The Review of Economic Studies*, 45, pp. 511–518.
Hutcheson, D., 2005, 'The R&D Crisis,' discussion paper (VLSI Research, Santa Clara California, U.S.A.).

Irwin, D. A. and Klenow, P. J., 1994, 'Learning-by-Doing Spillovers in the Semiconductor Industry,' *Journal of Political Economy*, 102, pp. 1200–1227.
ITRS, 2001, *The International Technology Roadmap for Semiconductors*, technical report, (Austin, Texas, U.S.A.) online at ITRS above.
Jorgenson, D. W., 2001, 'Information Technology and the U.S. Economy,' *American Economic Review*, 91, pp. 132.
Markoff, J., 28 July, 2011, 'Progress Hits Snag: Tiny Chips Use Outsize Power,' *The New York Times*.
Moore, G. E., 1965, 'Cramming More Components onto Integrated Circuits, *Electronics*, 38, pp. 114–117.
Moore, G. E., 1975, 'Progress in Digital Integrated Electronics,' *IEEE, IEDM Technical Digest*, pp. 11–13.
Nordhaus, W. D., 2001, 'The Progress of Computing,' discussion paper 1324, (Cowles Foundation, Yale University, New Haven, Connecticut, U.S.A.).
Oliner, S. D. and Sichel, D. E., 2002a, 'Information Technology and Productivity: Where Are We Now and Where Are We Going?,' *Finance and Economics Discussion Series 2002-29*, (Board of Governors of the Federal Reserve System Constitution Avenue, N.W., Washington, D.C., U.S.A.).
Oliner, S. D. and Sichel, D. E., 2002b, 'The Resurgence of Growth in the 1990's: Is Information Technology the Story?,' *Journal of Economic Perspectives*, 2000, pp. 3–22.
Oliner, S. D.; Sichel, D. E. and Stiroh, K. J., 2007, 'Explaining a Productive Decade,' *Finance and Economics Discussion Series 2007-63*, (Board of Governors of the Federal Reserve System Constitution Avenue, N.W., Washington, D.C., U.S.A.).
Patterson, D., 2010, 'The Trouble with Multicore,' *IEEE Spectrum*, 47, pp. 28–32.
Ronen, R.; Mendelson, A.; Lai, K.; Lu, S. L.; Pollack, F. and Shen, J. P., 2000, 'Coming Challenges in Microarchitecture and Architecture,' *Proceedings of the IEEE*, 89, pp. 325–340.
Semiconductor International, 2008, 'VLSI Research Ranks Top Equipment Vendors for 2007,' *www.semiconductor.net/article/CA6541940.html*.
Song, M., 2007, 'Measuring Consumer Welfare in the CPU Market: An Application of the Pure Characteristics Demand Model,' *RAND Journal Of Economics*, 38, pp. 429–446.
Stokey, N. L.; Lucas, R. E. and Prescott, E., 1989, *Recursive Methods in Economic Dynamics* (Harvard University Press, Cambridge Massachusetts, U.S.A.).
Sutton, J., 2001, *Technology and Market Structure: Theory and History, vol. 1* (The MIT Press, Cambridge Massachusetts, U.S.A.).