Title: Energy Efficient And Intelligent Processing-In-Memory for Data-Intensive Applications - From Device to Algorithm

Abstract: In-memory computing is becoming a promising solution to overcome the well-known 'memory-wall' challenge, through directly processing the data within memory where data is stored. Therefore, it will reduce massive power hungry data traffic between computing and memory units, leading to significant improvement of entire system performance and energy efficiency. Many different memory technologies have been explored for the design of processing-in-memory (PIM) or in-memory computing (IMC), such as emerging post-CMOS non-volatile memory (NVM), Static Random Access Memory (SRAM) or Dynamic RAM (DRAM), etc. In this talk, Dr. Deliang Fan, from Arizona State University (ASU), will present his recent research in energy efficient and intelligent cross-layer processing-in-memory design for data-intensive applications, spanning from memory device &circuit to in-memory computing architecture & algorithm co-optimization, to intrinsically integrate memory and processing units. In this talk, Dr. Fan will present the software-hardware co-design of PIM for different data-intensive applications, including deep neural network, data encryption, graph processing and bioinformatics.

Bio:

Dr. Deliang Fan is currently an Assistant Professor in the School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA. Before joining ASU in 2019, he was an assistant professor in Department of Electrical and Computer Engineering at University of Central Florida, Orlando, FL, USA. He received his M.S. and Ph.D. degrees, under the supervision of Prof. Kaushik Roy, in Electrical and Computer Engineering from Purdue University, West Lafayette, IN, USA, in 2012 and 2015, respectively.

Dr. Fan's primary research interests include Energy Efficient and High Performance Big Data Processing-In-Memory Circuit, Architecture and Algorithm, with applications in Deep Neural Network, Data Encryption, Graph Processing and Bioinformatics Acceleration-in-Memory system; Hardware-aware deep learning optimization; Brain-inspired (Neuromorphic) Computing; AI security. He has authored and co-authored 110+ peer-reviewed international journal/conference papers in above area. He is the receipt of best paper award of 2019 ACM Great Lakes Symposium on VLSI, 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), and 2017 IEEE ISVLSI. His research paper was also nominated as best paper candidate of 2019 Asia and South Pacific Design Automation Conference. He is also the technical area chair of DAC 2021, GLSVLSI 2019/2020/2021, ISQED 2019/2020/2021, and the financial chair of ISVLSI 2019. He served as technical reviewers for over 30 international journals/conferences, such as Nature Electronics, IEEE TNNLS, TVLSI, TCAD, TNANO, TC, TCAS, etc. He also served as the Technical Program Committee member of DAC, ICCAD, HPCA, MICRO, WACV, GLSVLSI, ISVLSI, ASP-DAC, etc. Please refer to https://dfan.engineering.asu.edu/ for more details