

Visualizing the Electrostatics of Material Interfaces to Nanoscale Dimensions

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Abstract:

Electrostatic barriers at material interfaces are the foundation of electronic and optoelectronic devices. Their nanoscale uniformity is of paramount concern with the continued scaling of devices into the sub 10 nm length scale and the development of futuristic nanoscale devices. The electrostatic barrier at metal-semiconductor and metal-insulator-semiconductor interfaces can be visualized using a scanning tunneling microscope in a mode called ballistic electron emission microscopy (BEEM). The BEEM method measures the fraction of the tip current that makes it from the metal into the semiconductor as a function of tip bias and position. The local barrier height is measured by acquiring tens of thousands of BEEM spectra on a grid of tip positions and then fitting them to extract the threshold for onset of BEEM current, which is a measure of the minimum energy the carriers need to surmount the barrier.

Computational modeling has been developed to extract information about the interface composition and inelastic and elastic scattering rates from the measured histograms. The modeling for the mixed Au/Ag system indicates a mixture of two barrier heights from the individual metal species as well as a skewing to higher energy from the scattering of the hot electrons. Incomplete silicide formation as well as nanometer thick dielectric layers have also been studied and provides new insight into their effects on the electrostatics that is not possible with conventional bulk transport measurements.